AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A processor, comprising:

a branch predictor to issue a first branch prediction at a branch point in a program;

a first circuit to ~~detect~~ identify an exact convergence point subsequent to said branch point in said program, said exact convergence point being a point at which a path mispredicted from said branch point converges with a correct path at a point of said correct path immediately following said branch point;

a scheduler to store instructions of said program subsequent to said branch point when said branch prediction is a misprediction, said scheduler to re-execute selected instructions of said program subsequent to said branch point, ~~only~~ upon ~~detecting~~ identifying said exact convergence point; and

a second circuit to track a first set of physical registers written subsequent to said branch point.

2. (Cancelled)

3. (Previously Presented) The processor of claim 1, wherein said selected instructions include a first set of instructions of said program whose source physical registers were tracked by said second circuit.

4. (Previously Presented) The processor of claim 1, wherein said scheduler further executes move instructions corresponding to a second set of instructions that write to said first set of physical registers prior to said exact convergence point.

5. (Previously Presented) The processor of claim 1, further comprising a recovery buffer to store said selected instructions outside said scheduler.

6. (Original) The processor of claim 1, wherein said branch predictor includes a branch target buffer to store target addresses indexed by branch locations in said program and wherein said first circuit includes an alternate target buffer coupled to said branch target buffer for determining said exact convergence point.

7. (Original) The processor of claim 6, wherein said branch predictor includes a branch confidence estimator to reverse a second branch prediction of low confidence to induce an induced exact convergence point.

8. (Original) The processor of claim 1, wherein said second circuit is a scoreboard including a set of flags corresponding to a set of physical registers, wherein one of said set of flags is set when a corresponding one of said set of physical registers is written between said branch point and said exact convergence point.

9. (Original) The processor of claim 8, wherein said one of said set of flags is cleared when said corresponding one of said set of physical registers is written subsequent to said exact convergence point.

10. (Currently Amended) A method, comprising:

     storing a set of instructions of a program subsequent to a mispredicted branch point;

tracking a set of physical registers written by a first selected subset of said set of instructions; and

re-executing a second selected subset of said set of instructions, subsequent to an exact convergence point, that use a first one of said set of physical registers as a source operand register, ~~only~~ upon ~~detecting~~ identifying said exact convergence point, said exact convergence point being a point at which a path mispredicted from said mispredicted branch point converges with a correct path at a point of said correct path immediately following said mispredicted branch point.

11. (Original) The method of claim 10, wherein said tracking includes setting a flag for a second one of said set of physical registers written on a mispredicted path subsequent to said mispredicted branch point.

12. (Original) The method of claim 11, further comprising clearing said flag when an instruction subsequent to said exact convergence point uses said second one of said set of physical registers as a source register.

13. (Original) The method of claim 10, wherein said storing includes placing said set of instructions in a restore buffer prior to reloading them into a scheduler.

14. (Original) The method of claim 10, wherein said restoring includes executing a corresponding move instruction for each of said first selected subset of said set of instructions.

15. (Original) The method of claim 10, further comprising reversing a branch prediction of a subsequent branch point to induce said exact convergence point.

16. (Currently Amended) A system, comprising:

      a processor including a branch predictor to issue a first branch prediction at a branch point in a program, a first circuit to ~~detect~~ identify an exact convergence point subsequent to said branch point in said program, said exact convergence point being a point at which a path mispredicted from said branch point converges with a correct path at a point of said correct path immediately following said branch point, a scheduler to store instructions of said program subsequent to said branch point when said branch prediction is a misprediction, said scheduler to re-execute selected instructions of said program subsequent to said branch point, ~~only~~ upon ~~detecting~~ identifying said exact convergence point, and a second circuit to track a first set of physical registers written subsequent to said branch point;

      an interface to couple said processor to input-output devices; and

      an audio input-output device coupled to said interface to receive audio data from said processor.

17. (Cancelled)

18. (Previously Presented) The system of claim 16, wherein said selected instructions include a first set of instructions of said program whose source physical registers were tracked by said second circuit.

19. (Previously Presented) The system of claim 16, wherein said scheduler further executes move instructions corresponding to a second set of instructions that write to said first set of physical registers prior to said exact convergence point.

20. (Previously Presented) The system of claim 16, further comprising a recovery buffer to store said selected instructions outside said scheduler.

21. (Original) The system of claim 16, wherein said branch predictor includes a branch target buffer to store target addresses indexed by branch locations in said program and wherein said first circuit includes an alternate target buffer coupled to said branch target buffer for determining said exact convergence point.

22. (Original) The system of claim 21, wherein said branch predictor includes a branch confidence estimator to reverse a second branch prediction of low confidence to induce an induced exact convergence point.

23. (Original) The system of claim 16, wherein said second circuit is a scoreboard including a set of flags corresponding to a set of physical registers, wherein one of said set of flags is set when a corresponding one of said set of physical registers is written between said branch point and said exact convergence point.

24. (Original) The system of claim 23, wherein said one of said set of flags is cleared when said corresponding one of said set of physical registers is written subsequent to said exact convergence point.

25. (Currently Amended) An apparatus, comprising:

      means for storing a set of instructions of a program subsequent to a mispredicted branch point;

      means for tracking a set of physical registers written by a first selected subset of said set of instructions; and

      means for re-executing a second selected subset of said set of instructions, subsequent to an exact convergence point, that use a first one of said set of physical registers as a source operand register, ~~only~~ upon ~~detecting~~ identifying said exact convergence point, said exact convergence point being a point at which a path mispredicted from said mispredicted branch point converges with a correct path at a point of said correct path immediately following said mispredicted branch point.

26. (Original) The apparatus of claim 25, wherein said means for tracking includes means for setting a flag for a second one of said set of physical registers written on a mispredicted path subsequent to said mispredicted branch point.

27. (Original) The apparatus of claim 26, further comprising means for clearing said flag when an instruction subsequent to said exact convergence point uses said second one of said set of physical registers as a source register.

28. (Original) The apparatus of claim 25, wherein said means for storing includes means for placing said set of instructions in a restore buffer prior to reloading them into a scheduler.

29. (Original) The apparatus of claim 25, wherein said means for restoring includes means for executing a corresponding move instruction for each of said first selected subset of said set of instructions.

30. (Original) The apparatus of claim 25, further comprising means for reversing a branch prediction of a subsequent branch point to induce said exact convergence point.

31. (New) The processor of claim 1, wherein said scheduler further uses move instructions to correct false data dependencies from the path mispredicted.

32. (New) The processor of claim 31, wherein using move instructions further comprises transforming write instructions to data dependent registers into move instructions.

33. (New) The processor of claim 1, wherein said scheduler further restores true data dependencies from false data dependencies.

34. (New) The processor of claim 33, wherein restoring true data dependencies further comprises correcting false data dependency values in physical registers.